Bahria University,

Karachi Campus



LAB EXPERIMENT NO.

**10**

LIST OF TASKS

|  |  |  |
| --- | --- | --- |
| TASK NO | OBJECTIVE | |
| **1** | Write a program in which take three inputs and do this logic: | |
| **2** | Verify the operation of NOT, AND, OR, NAND and NOR Gates using MultiSim and attach the circuit snapshots? | |
| **3** | Implement the following equations on MultiSim and verify through Truth Table. (Attach the circuit snapshots)  a. ABCD + A ( B + C) + BCD + ABD+ BC  b. (A+ B + C). (A + C+ D).(B+ C + D) | |
|  | |

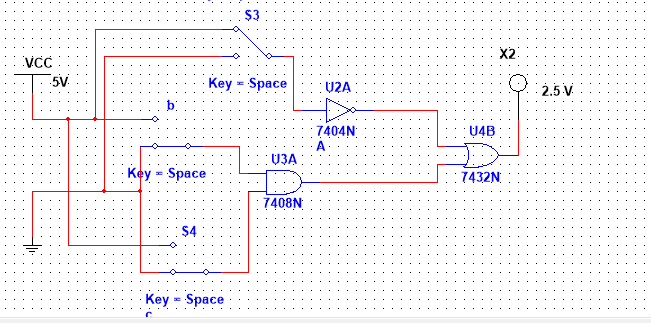
Submitted On:

Date: 19/12/2022

**Example :** Write a program in which take three inputs and do this logic:

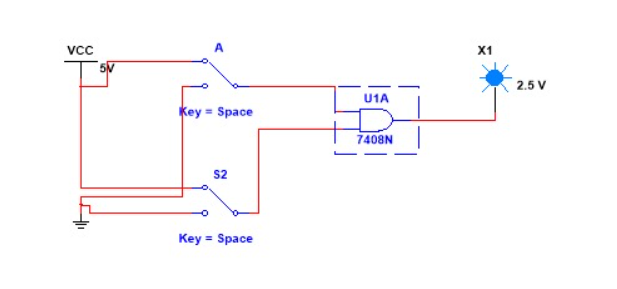
(BC)(!A)

**Output:**



**Task No 1 : Verify the operation of NOT, AND, OR, NAND and NOR Gates using MultiSim and attach the circuit snapshots.**

**AND Gate:**



**OR Gate**

Diagram

Description automatically generated with medium confidence**True:**

**False:**

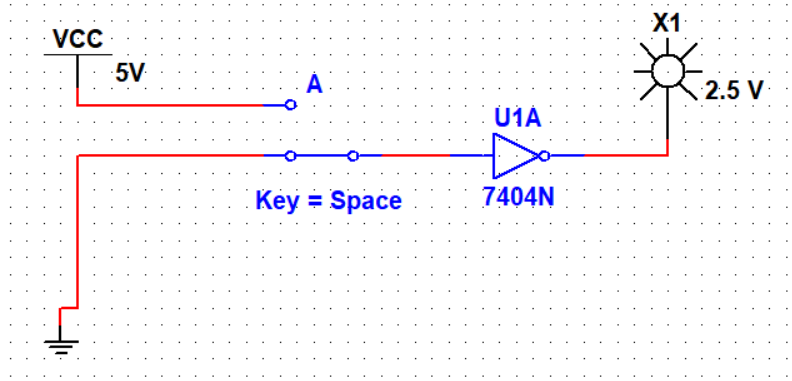
Diagram

Description automatically generated

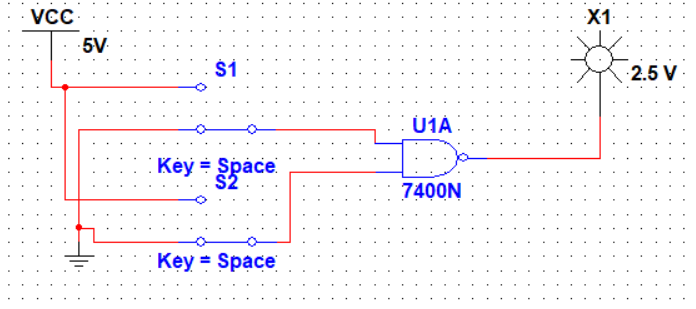
**NOT Gate:**

Chart, scatter chart

Description automatically generated**True:**

**False:**

**NAND Gate:**

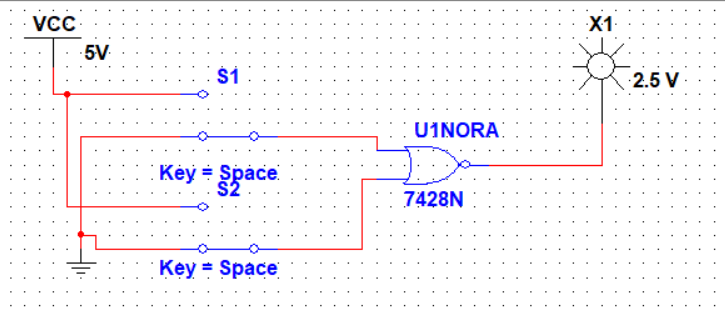
**True:**

Scatter chart

Description automatically generated with medium confidence**False:**

**NOR Gate:**

**True:**



**False:**

Diagram

Description automatically generated

**Task no 2:** Implement the following equations on MultiSim and verify through Truth Table. (Attach the circuit snapshots)

1. **ABCD + A ( B + C) + BCD + ABD+ BC**

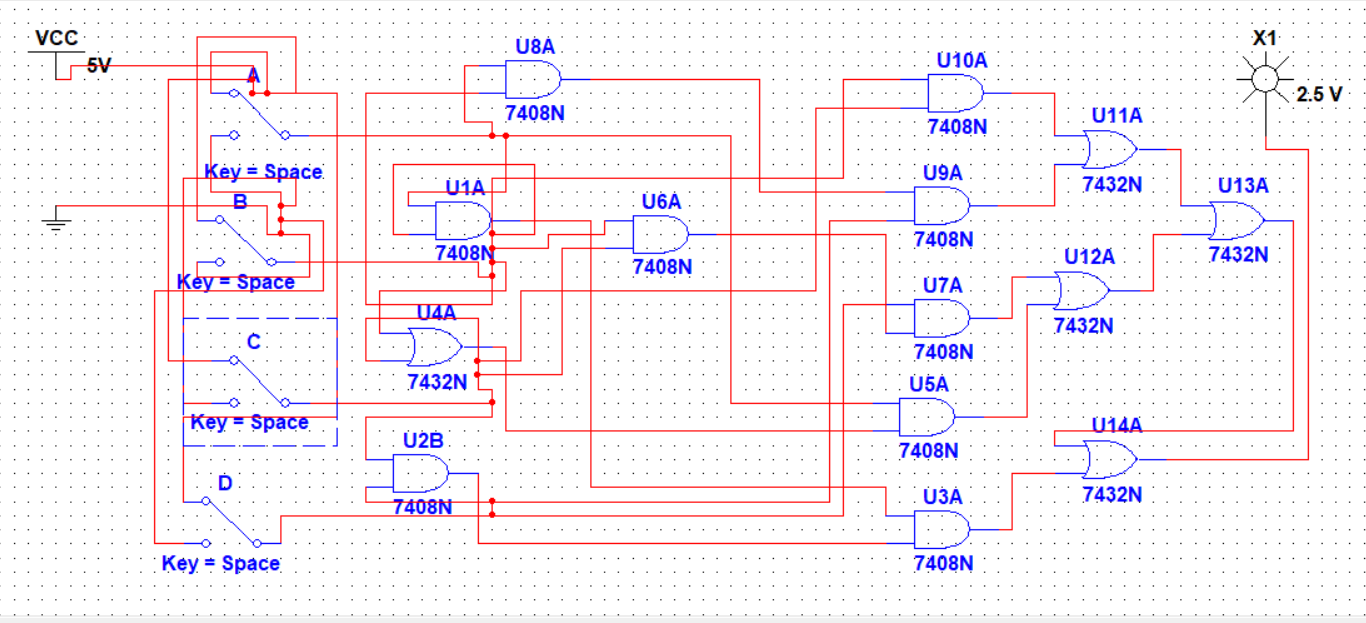
**Solution:**

**OBSERVATIONS / RESULTS & DISCUSSION:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Input: A** | **Input: B** | **Input: C** | **Input: D** | **B+C** | **ABCD** | **A(B+C)** | **BCD** | **ABD** | **BC** | **ABCD + A ( B + C) + BCD + ABD+ BC** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**Output :**

**True:**



**False:**

Diagram

Description automatically generated

b. (A+ B + C). (A + C+ D).(B+ C + D)

**Solution:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Input: A** | **Input:B** | **Input: C** | **Input: D** | **A+B+C** | **A+C+D** | **B+C+D** | (A+ B + C). (A + C+ D).(B+ C + D) |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Diagram, schematic

Description automatically generated

**Output :**